CLAIMS

1. A semiconductor device provided with:

an insulating tape substrate having through holes in the thickness direction;

a semiconductor element mounted on a top surface of the tape substrate with its back surface exposed upward and its active surface facing downward;

a sealing resin layer formed on the top surface of the tape substrate outside of the region in which the semiconductor device is mounted and sealing the area around the side surfaces of the semiconductor element;

metal interconnections formed on the bottom surface of the tape substrate and blocking the bottom ends of the through holes of the tape substrate to define bottom portions;

a solder resist layer covering the metal interconnections and the bottom surface of the tape substrate and having through holes in the thickness direction;

external connection terminals projecting from the bottom surface of the metal interconnections and filling, passing through, and projecting out downward through the through holes of the solder resist layer;

connection terminals extending downward from the active surface of the semiconductor element and inserted in the through holes of the tape substrate; and

a filler comprised of a conductive material filling the gaps between the connection terminals and the inside walls of the through holes of the tape substrate and electrically connecting the connection terminals and the metal interconnections.

2. A semiconductor device as set forth in claim 1, wherein the filler is formed using one of a low melting point metal and conductive paste.

3. A semiconductor device as set forth in claim 1, further provided with conductor columns passing through

said resin sealing layer and said tape substrate at a region where said resin sealing layer is formed, having top ends exposed at the top surface of the resin sealing layer, and having bottom ends electrically connected to said metal interconnection layer.

4. A semiconductor device as set forth in claim 1, further provided with, instead of said sealing resin layer, an insulating frame bonded to the top surface of the tape substrate other than at the region where said semiconductor element is mounted and surrounding the side surfaces of said semiconductor element with a gap and a resin sealing layer filling said gap and sealing the area around the side surfaces of said semiconductor element and further provided with conductor columns passing through said frame and said tape substrate at a region where said frame is formed, having top ends exposed at the top surface of the frame, and having bottom ends electrically connected to said metal interconnection layer.

5. A semiconductor device as set forth in claim 1, wherein the connection terminals extending downward from the active surface of the semiconductor element are bumps comprised of one of gold and copper.

6. A semiconductor device as set forth in claim 1, wherein the external connection terminals filling and passing through the openings of the solder resist layer are arranged in one of a peripheral and area array mode.

7. A semiconductor device as set forth in claim 1, wherein said filler is filled in the gap between said connection terminals and the through holes of said tape substrate up to a position of substantially the top ends of said through holes.

8. A semiconductor device as set forth in claim 1, wherein the top surface of said sealing resin layer and the back surface of said semiconductor element form substantially the same plane.

9. A multilayer semiconductor device comprised of

a plurality of semiconductor devices as set forth in claim 3 or 4 stacked in layers, wherein the semiconductor devices of each layer are connected with each other at the top ends of the conductor columns and the bottom ends of the external connection terminals.

10. A process of production of a semiconductor device comprising:

forming through holes in the thickness direction in a tape substrate having an area able to accommodate a plurality of semiconductor package units and provided at its bottom surface with a metal interconnection layer and a solder resist layer and in said solder resist layer;

filling a conductive material in the through holes of the tape substrate in amounts incompletely filling said through holes;

inserting connection terminals of a number of semiconductor elements required for forming a plurality of semiconductor package units into the corresponding through holes of the tape substrate and filling the gaps between the connection terminals and the inside walls of the through holes by said conductive material until about the top ends of the through holes;

bonding and mounting semiconductor elements on the top surface of the tape substrate;

forming a sealing resin layer covering the top surface of the tape substrate other than the regions where the semiconductor elements are mounted and sealing the area around the side surfaces of the semiconductor element;

grinding and polishing to a predetermined thickness the top part of the sealing resin layer and the back surface portions of the semiconductor elements; and

cutting the tape substrate into semiconductor package units to obtain individual semiconductor devices.

11. A process of production of a semiconductor

device as set forth in claim 10, further comprising forming other through holes passing through the tape substrate at positions corresponding to conductor columns when forming through holes in the tape substrate and forming conductor columns filling said other through holes and projecting out from the top surface of said tape substrate before forming said sealing resin layer.

12. A process of production of a semiconductor device as set forth in claim 10, further comprising bonding an insulating substrate provided with openings defining inner walls of frames to the top surface of said tape substrate, forming other through holes passing through the insulating substrate and the tape substrate at positions corresponding to conductor columns when forming through holes in the tape substrate, forming conductor columns filling said other through holes and projecting out from the top surface of said insulating substrate before mounting said semiconductor elements, and forming said sealing resin layer at the gaps after mounting the semiconductor elements.

13. A process of production of a semiconductor device as set forth in claim 10, further comprising performing electrical tests after forming said sealing resin layer and one of before and after said grinding and said polishing.

14. A process of production of a semiconductor device as set forth in claim 10, wherein the tape substrate able to accommodate said plurality of semiconductor package units is a disk shape.

15. A semiconductor device provided with:

an insulating tape substrate having metal interconnections on the top surface;

a semiconductor element mounted on a top surface of said tape substrate with its back surface exposed upward and its active surface facing downward;

a sealing resin layer formed on the top surface of the tape substrate, sealing the area around

the side surfaces of the semiconductor element, and filling the gap between the active surface of the semiconductor element and the top surface of the tape substrate; and

at least one of

conductor columns extending upward from the top surfaces of the metal interconnections, passing through the sealing resin layer at the area around the side surfaces of the semiconductor element, and having top ends exposed upward and

external connection terminals extending downward from the bottom surfaces of the metal interconnection, passing through the tape substrate, and projecting downward.

16. A semiconductor device as set forth in claim 15, wherein the top surface of said sealing resin layer and the back surface of said semiconductor element form substantially the same plane.

17. A process of production of a semiconductor device comprising:

preparing a tape substrate having an area able to accommodate a plurality of semiconductor package units and provided at its top surface with metal interconnections;

bonding connection terminals of active surfaces of a number of semiconductor elements required for forming the plurality of semiconductor package units to the top surfaces of the metal interconnections of said tape substrate to mount said semiconductor elements on the top surface of said tape substrate;

forming conductor columns with bottom ends bonded to the top surfaces of the metal interconnections;

forming a sealing resin layer sealing the area around the side surfaces of the semiconductor elements, including said metal interconnections and conductor columns, and filling the gaps between the active surfaces of the semiconductor elements and the top

surface of said tape substrate;

grinding and polishing to a predetermined thickness the top part of the sealing resin layer and the back surface portions of the semiconductor elements and exposing the top ends of the conductor columns upward; and

cutting the tape substrate into semiconductor package units to obtain individual semiconductor devices.

18. A process of production of a semiconductor device comprising:

preparing a tape substrate having an area able to accommodate a plurality of semiconductor package units, provided at its top surface with metal interconnections, having through holes in a thickness direction at positions corresponding to external connection terminals, and having bottom surfaces of said metal interconnections defining top ends of said through holes;

bonding connection terminals of active surfaces of a number of semiconductor elements required for forming the plurality of semiconductor package units to the top surfaces of the metal interconnections of said tape substrate to mount said semiconductor elements on the top surface of said tape substrate;

forming a sealing resin layer sealing the area around the side surfaces of the semiconductor elements, including said metal interconnections, and filling the gaps between the active surfaces of the semiconductor elements and the top surface of said tape substrate; then,

in either order,

grinding and polishing to a predetermined thickness the top part of the sealing resin layer and the back surface portions of the semiconductor elements and

forming external connection terminals extending downward from the bottom surfaces of said metal

interconnections defining the top ends of said through holes, filling said through holes, and projecting downward; and

cutting the tape substrate into semiconductor package units to obtain individual semiconductor devices.

19. A process of production of a semiconductor device comprising:

preparing a tape substrate having an area able to accommodate a plurality of semiconductor package units, provided at its top surface with metal interconnections, having through holes in a thickness direction at positions corresponding to external connection terminals, and having bottom surfaces of said metal interconnections defining top ends of said through holes;

bonding connection terminals of active surfaces of a number of semiconductor elements required for forming the plurality of semiconductor package units to the top surface of the metal interconnections of said tape substrate to mount said semiconductor elements on the top surface of said tape substrate;

forming conductor columns with bottom ends bonded to the top surfaces of the metal interconnections;

forming a sealing resin layer sealing the area around the side surfaces of the semiconductor elements, including said metal interconnections and conductor columns, and filling the gaps between the active surfaces of the semiconductor elements and the top surface of said tape substrate; then,

in either order,

grinding and polishing to a predetermined thickness the top part of the sealing resin layer and the back surface portions of the semiconductor elements and exposing the top ends of the conductor columns upward and

forming external connection terminals extending downward from the bottom surfaces of said metal

interconnections defining the top ends of said through holes, filling said through holes, and projecting downward; and

cutting the tape substrate into semiconductor package units to obtain individual semiconductor devices.

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20. A semiconductor device provided with:

a resin member of a predetermined thickness;

a semiconductor element sealed inside said resin member, having a back surface exposed at a top surface of said resin member, and having an active surface facing downward;

metal interconnections formed on the bottom surface of the resin member; and

connection terminals extending downward from the active surface of the semiconductor element and having bottom ends connected to top surfaces of said metal interconnections.

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21. A semiconductor device as set forth in claim 20, wherein the top surface of said sealing resin layer and the back surface of said semiconductor element form substantially the same plane.

22. A semiconductor device as set forth in claim 20, further provided with a solder resist layer covering the entire bottom surface of said resin member including said metal interconnections and connection bumps formed on the bottom surfaces of said metal interconnections, passing through said solder resist layer, and projecting downward.

23. A semiconductor device as set forth in claim 20, further provided with a plurality of conductor columns passing through said resin member from the top surface of said metal interconnections, extending upward, and having top ends exposed at the top surface of said resin member.

24. A semiconductor device as set forth in claim 23, wherein the side surfaces of the conductor columns

are exposed at the side surfaces of the resin member.

25. A semiconductor device as set forth in claim 20, further provided with a capacitor sealed inside said resin member and directly connected with said metal interconnections.

26. A semiconductor device as set forth in claim 25, wherein said capacitor is a multilayer ceramic capacitor including inner electrodes each having a surface being perpendicular to the thickness direction of said resin member.

27. A semiconductor device as set forth in claim 20, wherein an inorganic filler is dispersed in said resin member.

28. A multilayer semiconductor device comprised of a plurality of semiconductor devices as set forth in claim 23 stacked in layers, wherein the semiconductor devices of each layer are connected with each other at the top ends of the conductor columns and the bottom ends of the metal interconnections through connection bumps.

29. A parallel semiconductor device comprised of a plurality of semiconductor devices as set forth in claim 24 connected to each other at their side surfaces, wherein the semiconductor devices adjoining each other at their sides are electrically connected with each other at the side surfaces of the conductor columns exposed at the side surfaces of said resin member.

30. A multilayer parallel semiconductor device comprised of a plurality of semiconductor devices as set forth in claim 24 stacked in layers and connected to each other at their side surfaces, wherein the semiconductor devices of each layer are electrically connected with each other at the top ends of the conductor columns and the bottom ends of the metal interconnections through connection bumps and wherein the semiconductor devices adjoining each other at their sides are electrically connected with each other at the side surfaces of the conductor columns exposed at the side surfaces of said

resin member.

31. A process of production of a semiconductor device comprising:

mounting on the top surface of a metal substrate having an area able to accommodate a plurality of semiconductor package units semiconductor elements by turning the active surfaces of semiconductor elements downward and bonding front ends of connection terminals to the metal substrate;

covering the entire top surface of the metal substrate by a resin to form a resin member in which the semiconductor elements are sealed and to the bottom surface of which said metal substrate is bonded; then,

in either order,

grinding and polishing to a predetermined thickness the top part of the sealing resin layer and the back surface portions of the semiconductor elements and

patterning the metal substrate to form metal interconnections with top surfaces connected to the bottom ends of said connection terminals on the bottom surface of said resin member; and

cutting the resin member into semiconductor package units to obtain individual semiconductor devices.

32. A process of production of a semiconductor device as set forth in claim 31, further comprising forming conductor columns on the top surface of said metal substrate after forming said semiconductor elements on said metal substrate and before forming said resin member.

33. A process of production of a semiconductor device as set forth in claim 32, wherein said conductor columns are formed so that at least one of said top ends and side surfaces are exposed from said resin member.

34. A process of production of a semiconductor device as set forth in claim 31, further comprising,

after forming the metal interconnections on the bottom surface of said resin member, forming a solder resist layer covering the entire bottom surface of said resin member, including said metal interconnections, and connection bumps formed on the bottom surfaces of said metal interconnections, passing through the solder resist layer, and projecting downward.

35. A process of production of a semiconductor device comprising:

preparing a composite metal plate comprised of a metal substrate having an area able to accommodate a plurality of semiconductor package units and of an interconnection pattern comprised of a different type of metal from said metal substrate on its top surface;

mounting semiconductor elements on the top surface of the composite metal plate by turning the active surfaces of semiconductor elements downward and bonding front ends of connection terminals to the composite metal plate;

covering the entire top surface of the composite metal plate by a resin to form a resin member in which the semiconductor elements are sealed and to the bottom surface of which said composite metal plate is bonded; then,

in either order,

grinding and polishing to a predetermined thickness the top part of the resin member and the back surface portions of the semiconductor elements and

etching away the metal substrate of said composite metal plate and leaving the interconnection pattern so as to form metal interconnections comprised of said interconnection pattern with top surfaces connected to the bottom ends of said connection terminals on the bottom surface of the resin member; and

cutting the resin member into semiconductor package units to obtain individual

semiconductor devices.

36. A process of production of a semiconductor device as set forth in claim 35, further comprising forming conductor columns on the top surface of said metal substrate after forming said semiconductor elements on said composite metal plate and before forming said resin member.

37. A process of production of a semiconductor device as set forth in claim 36, wherein said conductor columns are formed so that at least one of said top ends and side surfaces are exposed from said resin member.

38. A process of production of a semiconductor device as set forth in claim 35, further comprising, after forming the metal interconnections on the bottom surface of said resin member, forming a solder resist layer covering the entire bottom surface of said resin member, including said metal interconnections, and connection bumps formed on the bottom surfaces of said metal interconnections, passing through the solder resist layer, and projecting downward.

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